

(9) CLAIMS

1. A semiconductor MOSFET structure having improved electrostatic discharge tolerance, the structure comprising:

a semiconductor substrate having an active device surface;

in said surface, a MOSFET source region and a MOSFET drain region separated by a channel region;

a P-type dopant region subjacent said drain region and having a dopant concentration and predetermined dimensions such inherent parasitic transistor gain of said MOSFET structure is increased.

2. The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set for increasing drain-to-substrate capacitance thereby.

3. The structure as set forth in claim 1 comprising:

said MOSFET is a N-channel MOSFET wherein said P-type dopant region has said dopant concentration and said predetermined dimensions set such that the MOSFET trigger voltage is decreased thereby.

4. The structure as set forth claim 1 wherein breakdown voltage of said parasitic transistor is tailored by depth of the P-type dopant region with respect to said surface

1 and said substrate.

2 5. The structure as set forth in claim 1 wherein said MOSFET is a N-channel
3 MOSFET located in a P-type dopant well in said epitaxial layer and surface concentration
4 of the dopant ions in the P-deep region is approximately an order of magnitude greater
5 than that of the dopant ions at the P-well 209 surface concentration.

6 6. The structure as set forth in claim 3 comprising:
7 a pair of MOSFETs, including a N-MOSFET, and a P-MOSFET, wherein said N-
8 MOSFET and said P-MOSFET are connected in a push-pull configuration.

9 7. The structure as set forth in claim 6 wherein the P-deep implant region in both the
10 P-MOSFET and the N-MOSFET reduces effective base width of parasitic transistors
11 therein via reduction of substrate-to-drain spacing.

12 8. An integrated circuit electrostatic discharge protection device for an IC Input-
13 output pad, the device comprising:
14 a N-MOSFET;
15 a P-MOSFET, wherein said N-MOSFET and P-MOSFET are connected in a push-
16 pull configuration with drain regions thereof connected to said Input-output pad; and
17 both said N-MOSFET and said P-MOSFET including a P-type dopant region
18 substantially subjacent respective the drain regions of each such that P-MOSFET
19 parasitic PNP transistor gain and N-MOSFET parasitic NPN transistor gain is increased

1 thereby.

2 9. An electrostatic discharge protection circuit for an IC having at least one I/O pad
3 and at least one VCC pad having a electrically grounded electrostatic discharge
4 protection device connected thereto, the circuit comprising:

5 a N-GCMOSFET having a first drain region connected to said I/O pad, a first gate
6 region connected to electrical ground, and a first source region connected to electrical
7 ground; and

8 a P-GCMOSFET having a second drain region connected to said I/O pad, a
9 second gate region connected to said VCC pad, and a second source region connected
10 to said VCC pad,

11 wherein said first drain region has a P-type dopant region substantially subjacent
12 thereto for enhancing parasitic NPN transistor gain thereof, and said second drain region
13 has a P-type dopant region substantially subjacent thereto for enhancing parasitic PNP
14 transistor gain thereof.

15 10. The circuit as set forth in claim 9 wherein when the I/O pad experiences an
16 electrostatic discharge event, the P-type drain, acting as the emitter, to source, acting as
17 base, forms a diode of the P-GCMOSFET that gets forward biased such that a first part
18 of Electrostatic discharge event current is shunted to ground via the P-epi and substrate
19 layers; a second part of the electrostatic discharge event current is shunted through the
20 parasitic PNP transistor of the GC-MOSFET to ground via the electrostatic discharge
21 protection device on the VCC pad as its parasitic NPN transistor is turned ON; a third

1 part of the Electrostatic discharge event current flows through N-GC-MOSFET, and a
2 parasitic NPN transistor of GC-MOSFET turns on during an electrostatic discharge event
3 and the third part of the electrostatic discharge current is shunted to ground.

4 11. A N-channel MOSFET structure for electrostatic discharge device, the structure
5 comprising:

6 a P-doped substrate having an epitaxial layer for forming active device elements
7 therein; and

8 within said epitaxial layer,

9 a N+ doped source region,

10 a N+ drain region,

11 a P-doped channel region between the source region and the drain
12 region,

13 a gate superjacent the channel,

14 an N-doped well region beneath said drain region having a width
15 dimension less than a width dimension of said drain region, and

16 a P-doped deep region, beneath said drain region and adjacent said well
17 region, having a dopant concentration greater than said P-doped channel region,

18 wherein said P-doped deep region increases gain of a parasitic lateral NPN
19 transistor formed by said source region, said channel region and said drain region and
20 lowers triggering voltage of said MOSFET.

21 12. A P-channel MOSFET structure for an electrostatic discharge protection circuit,

1 the structure comprising:

2 a P-doped substrate having an epitaxial layer;

3 an N-doped well in said epitaxial layer for forming active device elements therein;

4 and

5 within said N-doped well,

6 a P+ doped source region,

7 a P+ drain region,

8 a N-doped channel region between the source region and the drain

9 region,

10 a gate superjacent the channel, and

11 a P-doped deep region, beneath said drain region and adjacent said well

12 region,

13 wherein said P-doped deep region increases gain of a parasitic PNP transistor

14 formed by said drain region, N-doped well region and said epitaxial layer and lowers

15 triggering voltage of said MOSFET.

16 13. A MOSFET structure for an electrostatic discharge protection circuit, the structure
17 comprising:

18 a substrate having an epitaxial layer forming an active device surface;

19 at least two MOSFETs proximate said surface, each MOSFET having a first
20 dopant type drain region wherein said drain regions are adjacent and separated by a
21 region of said surface and forming diode poles thereby; and

22 a second dopant type deep region at said region of the surface, wherein said

1 deep region has a depth from said surface into said epitaxial layer greater than a depth
2 of each of said drain regions such that an electrostatic discharge spike causes a diode
3 breakdown to the epitaxial layer before affecting the MOSFETs.

4 14. The structure as set forth in claim 13 wherein said deep region has a
5 predetermined P-type ion concentration and predetermined dimensions such that an
6 electrostatic discharge spike at said drain will cause a diode breakdown through epitaxial
7 layer and substrate before affecting the MOSFETs.

8 15. A MOSFET structure for an electrostatic discharge protection circuit employing an
9 SCR, the structure located in an epitaxial layer of a first dopant type of a substrate, said
10 epitaxial layer having an active device surface, the structure comprising:

11 a first MOSFET of a second dopant type located proximate said surface and
12 having a first drain region of the second dopant type;

13 a second MOSFET of the second dopant type and located proximate said surface
14 and having a second drain region of the second dopant type proximate said first drain
15 region;

16 a drain contact electrically connecting said first drain region and said second
17 drain region;

18 a surface contact region abutting said drain contact and separating said first drain
19 region said second drain region, said surface region having said first dopant type;

20 subjacent the surface contact region and within said epitaxial layer, a well of said
21 second dopant type, wherein said well is subjacent both said first drain region and said

1 second drain region; and

2 within said well, a deep region of P-type ion dopant, wherein said deep region is
3 subjacent both said first drain region, said second drain region, and said surface contact
4 region,

5 wherein said deep region dimensions and concentration of the P-type ion are
6 predetermined for achieving a desired SCR punch-through voltage via tuning breakdown
7 fields and improving structure inherent bipolar transistor gain accordingly.

8 16. The structure as set forth in claim 15 wherein punch-through voltage of the SCR
9 is controlled by the spacing between the deep region and P-wells.

10 17. The structure as set forth in claim 15 wherein during a positive electrostatic
11 discharge spike to an I/O pad associated with the structure, the SCR being in parallel
12 with the N-channel MOSFETs conduct a significant amount of current, enhancing
13 electrostatic discharge protection.

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15 18. A BiCMOS technology N-MOSFET structure for electrostatic discharge protection
16 circuits, the structure comprising:

17 a P ion doped substrate;

18 an N ion doped epitaxial layer superjacent said substrate, said epitaxial layer

19 having an upper surface distal from said substrate;

20 a buried isolation layer;

21 a P ion doped well subjacent in said upper surface;

1 a N+ ion doped source region subjacent said surface;
2 a N+ ion doped drain region subjacent said surface;
3 a region of said well forming a P ion channel region at said surface between said
4 source region and said drain region;
5 a gate structure superposing said channel region; and
6 subjacent said drain region and within said well, a P ion doped deep region, said
7 deep region having an ion concentration greater than ion concentration of said well,
8 such that lateral bipolar parasitic NPN transistor of said structure is provided with
9 increased gain by the deep region.

10 19. A BiCMOS technology P-MOSFET structure for electrostatic discharge protection
11 circuits, the structure comprising:

12 a P ion doped substrate;
13 an N ion doped epitaxial layer superjacent said substrate, said epitaxial layer
14 having an upper surface distal from said substrate;
15 a buried isolation layer;
16 a N ion doped well subjacent in said upper surface;
17 a P+ ion doped source region subjacent said surface;
18 a P+ ion doped drain region subjacent said surface;
19 a region of said well forming a N ion channel region at said surface between said
20 source region and said drain region;
21 a gate structure superposing said channel region; and
22 subjacent said drain region and within said well, a P ion doped deep region, said

1 deep region having an ion concentration substantially equal to or greater than ion
2 concentration of said drain region,
3 such that vertical bipolar parasitic PNP transistor of said structure is provided with
4 increased gain by the deep region.

5 20. A BiCMOS technology structure for a push-pull Input-output electrostatic
6 discharge protection circuit employing an SCR, the structure located in an epitaxial layer
7 of a first dopant type of a substrate of a second dopant type, said epitaxial layer having
8 an active device surface, the structure comprising:

9 a first dopant type buried layer segregating said epitaxial layer and said
10 substrate;

11 a second dopant type first well within said epitaxial layer and subjacent said
12 surface;

13 a second dopant type second well within said epitaxial layer and subjacent said
14 surface;

15 a first dopant type third well within said epitaxial layer and subjacent said surface,
16 such that third well is adjacently between said first well and said second well;

17 a first MOSFET of the first dopant type located within said first well proximate said
18 surface and having a first drain region of the first dopant type and having a
19 predetermined drain width for superjacently spanning a first area of said surface
20 encompassing surface regions of both said first well and said third well;

21 a second MOSFET of the first dopant type and located within said second well
22 proximate said surface and having a second drain region of the first dopant type and

1 having a predetermined drain width for superjacent spanning a second area of said
2 surface encompassing surface regions of both said third well and said second well;
3 a drain contact electrically connecting said first drain region and said second
4 drain region;
5 a surface contact region abutting said drain contact and separating said first drain
6 region said second drain region, said surface region having said second dopant type;
7 within said third well, a deep region of P-type ion dopant, wherein said deep
8 region is subjacent both said first drain region, said second drain region, and said
9 surface contact region,
10 wherein said deep region dimensions and concentration of the P-type ion are
11 predetermined for achieving a desired SCR punch-through voltage via tuning breakdown
12 fields and improving structure inherent bipolar transistor gain accordingly.

13 21. An extended drain N-channel MOSFET structure comprising:

14 a P-type substrate;
15 in said substrate at least one MOSFET structure having extended and enhanced
16 drain region devices for providing reduced on-resistance at a surface region of said
17 substrate, said MOSFET structure including an N+ doped drain region in an N-type well
18 region; and
19 a P-deep region subjacent the N-well containing the drain region, said P-deep
20 region having geometry and a dopant concentration such that said P-deep region
21 increases gain of a parasitic lateral NPN transistor and lowers triggering voltage of said
22 MOSFET, improving electrostatic discharge tolerance thereby.